

WHAT IS CLAIMED IS:

- 1     1.     A memory cell comprising:  
2             a p-well area having at least one NMOS transistor formed therein, the NMOS  
3     transistor having an NMOS active area; and  
4             an n-well area having at least one PMOS transistor formed therein; and  
5             wherein the memory cell has a long side and a short side, the long side being at  
6     least twice as long as the short side, a longitudinal axis of the p-well being parallel to the  
7     short side.
- 1     2.     The memory cell of claim 1, wherein the memory cell is a 6T-SRAM cell.
- 1     3.     The memory cell of claim 2, wherein maximum resistance between cells p-well to  
2     p-well strap contact is less than 4000 ohm.
- 1     4.     The memory cell of claim 2, wherein maximum distance between cells p-well to  
2     p-well low resistance strap is less than 3.6  $\mu\text{m}$ .
- 1     5.     The memory cell of claim 2, wherein the p-well area is less than about 65% of the  
2     memory cell.

- 1 6. The memory cell of claim 2, wherein the distance from the n-well area to the  
2 NMOS active area is less than about 75 nm.
- 1 7. The memory cell of claim 2, wherein the NMOS active region is less than about  
2 25% of the memory cell.
- 1 8. The memory cell of claim 2, wherein the short side is less than about 0.485  $\mu\text{m}$ .
- 1 9. The memory cell of claim 1, wherein the memory cell is an 8T-SRAM cell.
- 1 10. The memory cell of claim 9, wherein maximum resistance between cells p-well to  
2 p-well strap contact is less than 4000 ohm.
- 1 11. The memory cell of claim 9, wherein maximum distance between cells p-well to  
2 p-well low resistance strap is less than 3.6  $\mu\text{m}$ .
- 1 12. The memory cell of claim 9, wherein the p-well area is less than about 75% of the  
2 memory cell.
- 1 13. The memory cell of claim 9, wherein the distance from the n-well area to the  
2 NMOS active area is less than about 100 nm.

- 1 14. The memory cell of claim 9, wherein the NMOS active region is less than about  
2 33% of the memory cell.
- 1 15. The memory cell of claim 9, wherein the short side is less than about 0.745  $\mu\text{m}$ .
- 1 16. The memory cell of claim 1, wherein the n-well is a deep n-well.
- 1 17. The memory cell of claim 1, wherein the p-well substantially encircles the n-well.
- 1 18. The memory cell of claim 1, wherein the memory cell includes a plurality of  $V_{ss}$   
2 lines, the plurality of  $V_{ss}$  lines being located on one or more metal layers.
- 1 19. The memory cell of claim 1, wherein the memory cell has an area of less than  
2 about 0.4  $\mu\text{m}^2$ , at least one of the PMOS transistors or the NMOS transistors have a gate  
3 thickness less than about 1000 Å.
- 1 20. The memory cell of claim 1, wherein the NMOS transistor has a gate layer and a  
2 gate dielectric layer and the gate dielectric layer having one or more layers and at least  
3 one layer comprising  $\text{SiO}_2$ , nitrided oxide, nitrogen content oxide, SiON, metal oxide,  
4 high K dielectric, or a combination thereof.

1 21. The memory cell of claim 1, wherein the memory cell includes at least one  
2 pull-down transistor having a gate width of less than about 40 nm and a gate dielectric  
3 thickness of less than 13 Å.

1 22. The memory cell of claim 1, wherein the memory cell has a maximum storage  
2 capacitance of less than about 0.5 femto-farad.

1 23. The memory cell of claim 1, wherein the memory cell includes at least one bit  
2 line, each bit line being parallel to the longitudinal axis of the p-well.

1 24. The memory cell of claim 1, wherein the memory cell is formed on a substrate  
2 comprising bulk-Si, SiGe, strain-Si, SOI, non-bulk Si, or a combination thereof.

1 25. The memory cell of claim 1, wherein the memory cell includes at least one bit  
2 line, each bit line having at least one of a  $V_{cc}$  line or a  $V_{ss}$  line thereof adjacent the bit  
3 line.

1 26. The memory cell of claim 1, wherein the memory cell includes a plurality of  
2 metal layers, and the memory cell includes a bit line and a complementary bit line, the bit  
3 line and the complementary bit line being on different metal layers.

1     27.     A memory cell comprising:     ✓  
2             a p-well area having a first portion and a second portion, the first portion having a  
3     first pass-gate transistor and a first pull-down transistor, the second portion having a  
4     second pass-gate transistor and a second pull-down transistor; and  
5             an n-well area positioned between the first portion and the second portion, the  
6     n-well area having a first pull-up transistor and a second pull-up transistor;  
7             wherein  
8             the memory cell has a long side and a short side, the long side being at  
9             least twice as long as the short side, the short side being less than 0.485  $\mu\text{m}$ ,  
10            and a longitudinal axis of the p-well being parallel to the short side  
11            the gate of the first pass-gate transistor is electrically coupled to a  
12            word line;  
13            the source of the first pass-gate transistor is electrically coupled to a  
14            bit line;  
15            the drain of the first pass-gate transistor is electrically coupled to the  
16            drain of the first pull-down transistor;

17                   the source of the first pull-down transistor is electrically coupled to a  
18                    $V_{ss}$  line;  
19                   the drain of the first pass-gate transistor, the drain of the first pull-up  
20                   transistor, the drain of the first pull-down transistor, the gate of the second  
21                   pull-down transistor, and second pull-up transistor are electrically coupled;  
22                   the drain of the second pass-gate transistor, the drain of the second  
23                   pull-up transistor, the drain of the second pull-down transistor, the gate of the  
24                   first pull-down transistor, and first pull-up transistor are electrically coupled;  
25                   the source of the first pull-up transistor is electrically coupled to a  $V_{cc}$   
26                   line;  
27                   the source of the second pull-up transistor is electrically coupled to the  
28                    $V_{cc}$  line;  
29                   the gate of the second pass-gate transistor is electrically coupled to the  
30                   word line;  
31                   the source of the second pass-gate transistor is electrically coupled to a  
32                   bit line bar;

33                   the drain of the second pass-gate transistor is electrically coupled to  
34                   the drain of the second pull-down transistor;  
35                   the source of the second pull-down transistor is electrically coupled to  
36                   the  $V_{ss}$  line;  
37                   a first axis along the source-to-drain direction of the first pass-gate  
38                   transistor is substantially parallel to the shorter side of the memory cell;  
39                   a second axis along the source-to-drain direction of the first pull-down  
40                   transistor is substantially parallel to the shorter side of the memory cell;  
41                   a third axis along the source-to-drain direction of the first pull-up  
42                   transistor is substantially parallel to the shorter side of the memory cell;  
43                   a fourth axis along the source-to-drain direction of the second  
44                   pass-gate transistor is substantially parallel to the shorter side of the memory  
45                   cell;  
46                   a fifth axis along the source-to-drain direction of the second pull-down  
47                   transistor is substantially parallel to the shorter side of the memory cell; and  
48                   a sixth axis along the source-to-drain direction of the second pull-up  
49                   transistor is substantially parallel to the shorter side of the memory cell.

- 1 28. The memory cell of claim 27, wherein resistance between a p-well to a p-well  
2 strap contact is less than about 4000 ohm.
- 1 29. The memory cell of claim 27, wherein the distance from a p-well to a p-well strap  
2 contact is less than about 3.6 um.
- 1 30. The memory cell of claim 27, wherein the p-well area is less than about 65% of  
2 the memory cell.
- 1 31. The memory cell of claim 27, wherein the distance of the n-well area to the  
2 NMOS active area is less than about 75 nm.
- 1 32. The memory cell of claim 27, wherein the NMOS active region is less than about  
2 25% of the memory cell.
- 1 33. The memory cell of claim 27, wherein the n-well is a deep n-well.
- 1 34. The memory cell of claim 27, wherein the p-well substantially encircles the  
2 n-well.
- 1 35. The memory cell of claim 27, wherein the memory cell includes a plurality of  $V_{ss}$   
2 lines, the plurality of  $V_{ss}$  lines being located on one or more metal layers.



1 36. The memory cell of claim 27, wherein the memory cell has an area of less than  
2 about  $0.4 \mu\text{m}^2$ , at least one of the PMOS transistors or the NMOS transistors have a gate  
3 thickness less than about  $1000 \text{ \AA}$ , and the memory cell includes at least one pull-down  
4 transistor having a gate width of less than about 40 nm.

1 37. The memory cell of claim 27, wherein at least one of the first pull-up transistors  
2 and the second pull-up transistor has a gate layer and a gate oxide layer and the gate  
3 oxide layer having one or more layers and at least one layer comprising  $\text{SiO}_2$ , nitrided  
4 oxide, nitrogen content oxide, SiON, metal oxide, high K dielectric, or a combination  
5 thereof.

1 38. The memory cell of claim 27, wherein at least one of the first pull-down transistor  
2 and the second pull-down transistor have a gate width of less than about 40 nm and a gate  
3 oxide thickness of less than  $13 \text{ \AA}$ .

1 39. The memory cell of claim 27, wherein the memory cell has a maximum storage  
2 capacitance of less than about 0.5 femto-farad.

1 40. The memory cell of claim 27, wherein each bit line is parallel to the longitudinal  
2 axis of the p-well.

1 41. The memory cell of claim 27, wherein the memory cell is formed on a substrate  
2 comprising bulk-Si, SiGe, strain-Si, SOI, non-bulk Si, or a combination thereof.

1 42. The memory cell of claim 27, wherein the memory cell includes at least one bit  
2 line, each bit line having a  $V_{cc}$  line and a  $V_{ss}$  line adjacent the bit line.

1 43. The memory cell of claim 27, wherein the memory cell includes a plurality of  
2 metal layers, and the memory cell includes a bit line and a complementary bit line, the bit  
3 line and the complementary bit line being on different metal layers.



18                   the source of the third pass-gate transistor is electrically coupled to a  
19                   second bit line;  
20                   the drain of the first pass-gate transistor is electrically coupled to the  
21                   drain of the first pull-down transistor;  
22                   the source of the first pull-down transistor is electrically coupled to a  
23                    $V_{ss}$  line;  
24                   the source of the second pull-down transistor is electrically coupled to  
25                   a  $V_{ss}$  line;  
26                   the drain of the first pass-gate transistor, the drain of the first  
27                   pull-down transistor, the drain of the first pull-up transistor, the gate of the  
28                   second pull-down transistor, the gate of the second pull-up transistor, and the  
29                   drain of the third pass-gate transistor are electrically coupled;  
30                   the drain of the fourth pass-gate transistor, the drain of the second  
31                   pull-down transistor, the drain of the second pull-up transistor, the gate of the  
32                   first pull-down transistor, the gate of the first pull-up transistor, and the drain  
33                   of the second pass-gate transistor are electrically coupled;

34                   the source of the first pull-up transistor is electrically coupled to a  $V_{cc}$   
35           line;  
36                   the source of the second pull-up transistor is electrically coupled to the  
37            $V_{cc}$  line;  
38                   the source of the second pass-gate transistor is electrically coupled to a  
39           first complementary bit line;  
40                   the source of the fourth pass-gate transistor is electrically coupled to a  
41           second complementary bit line;  
42                   a first axis along the source-to-drain direction of the first pass-gate  
43           transistor is substantially parallel to the shorter side of the memory cell;  
44                   a second axis along the source-to-drain direction of the first pull-down  
45           transistor is substantially parallel to the shorter side of the memory cell;  
46                   a third axis along the source-to-drain direction of the first pull-up  
47           transistor is substantially parallel to the shorter side of the memory cell;  
48                   a fourth axis along the source-to-drain direction of the second  
49           pass-gate transistor is substantially parallel to the shorter side of the memory  
50           cell;

51                   a fifth axis along the source-to-drain direction of the second pull-down  
52           transistor is substantially parallel to the shorter side of the memory cell;  
53                   a sixth axis along the source-to-drain direction of the second pull-up  
54           transistor is substantially parallel to the shorter side of the memory cell;  
55                   a seventh axis along the source-to-drain direction of the third pass-gate  
56           transistor is substantially parallel to the shorter side of the memory cell; and  
57                   an eighth axis along the source-to-drain direction of the fourth pass-gate  
58           transistor is substantially parallel to the shorter side of the memory cell.

1    45.    The memory cell of claim 44, wherein resistance between a p-well to a p-well  
2    strap contact is less than about 4000 ohm.

1    46.    The memory cell of claim 44, wherein the distance from a p-well to a p-well strap  
2    contact is less than about 3.6um.

1    47.    The memory cell of claim 44, wherein the p-well area is less than about 75% of  
2    the memory cell.

1    48.    The memory cell of claim 44, wherein the distance of the n-well area to the  
2    NMOS active area is less than about 100 nm.

1 49. The memory cell of claim 44, wherein the NMOS active region is less than about  
2 33% of the memory cell.

1 50. The memory cell of claim 44, wherein the n-well is a deep n-well.

1 51. The memory cell of claim 44, wherein the p-well substantially encircles the  
2 n-well.

1 52. The memory cell of claim 44, wherein the memory cell includes a plurality of  $V_{ss}$   
2 lines, the plurality of  $V_{ss}$  lines being located on one or more metal layers.

1 53. The memory cell of claim 44, wherein the memory cell has an area of less than  
2 about  $1.2 \mu\text{m}^2$ , at least one of the PMOS transistors or the NMOS transistors have a gate  
3 thickness less than about 1000 Å.

1 54. The memory cell of claim 44, wherein at least one of the first pull-up transistors  
2 and the second pull-up transistor has a gate layer and a gate oxide layer and the gate  
3 oxide layer having one or more layers and at least one layer comprising  $\text{SiO}_2$ , nitrided  
4 oxide, nitrogen content oxide, SiON, metal oxide, high K dielectric, or a combination  
5 thereof.

1 55. The memory cell of claim 44, wherein at least one of the first pull-down transistor  
2 and the second pull-down transistor have a gate width of less than about 40 nm and a gate  
3 oxide thickness of less than 13 Å.

1 56. The memory cell of claim 44, wherein the memory cell has a maximum storage  
2 capacitance of less than about 1 femto-farad.

1 57. The memory cell of claim 44, wherein each bit line is parallel to the longitudinal  
2 axis of the p-well.

1 58. The memory cell of claim 44, wherein the memory cell is formed on a substrate  
2 comprising bulk-Si, SiGe, strain-Si, SOI, non-bulk Si, or a combination thereof.

1 59. The memory cell of claim 44, wherein the memory cell includes at least one bit  
2 line, each bit line having at least one of a  $V_{cc}$  line or a  $V_{ss}$  line adjacent the bit line.



- 1 60. A method of forming a memory cell, the method comprising the steps of:
- 2 providing a p-type substrate having a p-well;
- 3 forming an n-well in the p-type substrate;
- 4 forming in the n-well a first pull-up transistor and a second pull-up transistor;
- 5 forming in the p-well a first pass-gate transistor, a second pass-gate transistor, a
- 6 first pull-down transistor, and a second pull-down transistor;
- 7 wherein the memory cell has a shorter side and a longer side, the longer side
- 8 being at least twice as long as the shorter side, and wherein the source-to-drain axis of
- 9 each transistor is parallel to the shorter side.
- 1 61. The method of 60, wherein the n-well is less than about 65% of the memory cell.
- 1 62. The method of 60, wherein maximum distance between any p-well location to a
- 2 p-well low resistance strap is less than about 3.6  $\mu\text{m}$ .
- 1 63. The method of 60, wherein the distance between an NMOS active area and the
- 2 n-well is less than about 75 nm.
- 1 64. The method of 60, wherein the shorter side is less than about 0.485  $\mu\text{m}$ .

- 1 65. The method of 60, wherein the n-well is a deep n-well.

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1 66. A method of forming a memory cell, the method comprising the steps of:  
2 providing a p-type substrate having a p-well;  
3 forming an n-well in the p-type substrate;  
4 forming in the n-well a first pull-up transistor and a second pull-up transistor;  
5 forming in the p-well a first pass-gate transistor, a second pass-gate transistor, a  
6 third pass-gate transistor, a fourth pass-gate transistor, a first pull-down transistor, and a  
7 second pull-down transistor;  
8 wherein the memory cell has a shorter side and a longer side, the longer side  
9 being at least twice as long as the shorter side, and wherein the source-to-drain axis of  
10 each transistor is parallel to the shorter side.

1 67. The method of 65, wherein the n-well is less than about 75% of the memory cell.

1 68. The method of 65, wherein maximum distance between any p-well location to a  
2 p-well low resistance strap is less than about 3.6  $\mu\text{m}$ .

1 69. The method of 65, wherein the distance between an NMOS active area and the  
2 n-well is less than about 100 nm.

1 70. The method of 65, wherein the shorter side is less than about 0.745  $\mu\text{m}$ .

- 1 71. The method of 65, wherein the n-well is a deep n-well.